

WHAT IS CLAIMED IS:

1 1. A trench field effect transistor formed on a silicon substrate,
2 the trench transistor comprising:
3 a trench extending into the substrate;
4 a dielectric layer formed on walls and bottom of the trench; and
5 a gate conductive material substantially filling the trench,
6 wherein, the dielectric layer comprises a gate oxide layer grown at a
7 temperature above about 1,100 °C to result in the gate oxide layer having a
8 thickness that is substantially uniform, the gate oxide layer having substantially
9 uniform stress.

1 2. The trench transistor of claim 1 wherein the dielectric layer
2 further comprises:
3 a silicon nitride layer disposed on the gate oxide layer; and
4 a second oxide layer disposed between the silicon nitride layer and
5 the gate conductive material.

1 3. The trench transistor of claim 2 wherein the gate oxide layer
2 has a first thickness of at least about 300 Å, the silicon nitride layer has a second
3 thickness of about 120Å, and the second oxide layer has a third thickness of about
4 50 Å.

1 4. A trench field effect transistor formed on a silicon substrate,
2 the trench transistor comprising:
3 a trench extending into the substrate;
4 a first oxide layer thermally grown on walls and bottom of the
5 trench;

6 a silicon nitride layer disposed on the first oxide layer;
 7 a second oxide layer disposed on the silicon nitride layer; and
 8 a gate conductive material substantially filling the trench.

1 5. The trench transistor of claim 4 wherein the first oxide layer is
 2 grown at a temperature of at least about 1,100°C.

1 6. The trench transistor of claim 5 wherein the first oxide has a
 2 thickness of about 300Å.

1 7. The trench transistor of claim 6 wherein the silicon nitride
 2 layer has a thickness of about 120Å.

1 8. The trench transistor of claim 7 wherein the second oxide
 2 layer has a thickness of about 50Å.

1 9. A method of forming a gate dielectric layer of a trench field-
 2 effect transistor, the method comprising the steps of:

- 3 (a) forming a trench in silicon on a substrate; and
 4 (b) heating the substrate to at least about 1,100 °C to form a layer
 5 of silicon oxide at least about 100 Å thick inside the trench.

1 10. The method of claim 9 further comprising the steps of:
 2 (c) forming a layer of silicon nitride on the layer of silicon oxide;
 3 and
 4 (d) forming a second layer of oxide on the layer of silicon nitride.

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1 11. The method of claim 10 wherein the layer of silicon nitride is
2 about 120Å thick.

1 12. The method of claim 10 wherein a low-pressure chemical-
2 vapor deposition process is used to form a conformal layer of silicon nitride.

CVD
(Si_3N_4)

1 13. The method of claim 11 wherein the second layer of oxide is
2 about 50Å thick.

1 14. A method of forming a gate dielectric layer of a trench field-
2 effect transistor, the method comprising:
3 (a) forming a trench in silicon on a substrate;
4 (b) heating the substrate to at least about 1,100 °C to form a layer
5 of silicon oxide at least about 100Å thick;
6 (c) forming a conformal layer of silicon nitride about 120Å thick
7 on the layer of silicon oxide by a low-pressure chemical-vapor deposition process;
8 and
9 (d) growing a second layer of oxide about 50Å thick on the layer
10 of silicon nitride.

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